Seat No.

T.E. (Electronics) (Part - I) (Semester - V) (Revised) Examination, May - 2017
DIGITAL COMMUNICATION
Sub. Code : 66284

Day and Date : Friday, 19 - 05 - 2017   **Total Marks : 100**
Time : 10.00 a.m. to 1.00 p.m.

Instructions :
1) All questions are compulsory.
2) Figures to the right indicate full marks.
3) Assume suitable data if necessary.

Q1) Solve any two: **[18]**

a) The probability that India wins a cricket match against Australia is known to be 2/5. If India and Australia play 3 matches what is the probability that

   i) India will lose all the three matches.

   ii) India will win atleast one match.

   iii) India will win all the matches.

   iv) India will win atmost one match.

b) State an expression for Gaussian distribution function. Also derive the expression for complementary error function.

c) A random variable has a distribution funciton given by

$$F_x(x)=\begin{cases} 0 & -\infty<x\le-10 \\ \dfrac{1}{6} & -10<x\le-5 \\ \dfrac{1}{15}x+\dfrac{1}{2} & -5<x<5 \\ \dfrac{5}{6} & 5\le x<10 \\ 1 & 10<x<\infty \end{cases}$$

Draw the distribution function associated with the random variable.

Q2) Solve any two: [16]

a) Explain pulse code modulation technique with the help of block diagram. Derive an expression for S/N ratio.

b) Draw and explain with block diagram the linear Delta modulation.

c) Explain in detail Uniform quantization.

Q3) Solve any two: [16]

a) What is PDF? Explain its properties in brief with proof.

b) Represent the data 1 0 0 1 1 0 1 0 0 using following data formats with the help of waveforms.
   i) Unipolar RZ
   ii) Polar RZ
   iii) M-ary
   iv) AMI

c) Explain scrambler and unscrambler using tapped shift register with feedback arrangement.

Q4) Solve any two: [16]

a) With neat block diagram explain BPSK transmitter and receiver.

b) Draw and explain ASK signalling scheme.

c) Explain transmitter and receiver of FSK with neat diagram and waveform.

Q5) Solve any two: [16]

a) What is equalization? Draw and explain Adaptive equalizer for data transmission.

b) Explain eye pattern with suitable diagram.

c) Discuss properties and application of matched filter.

Q6) Solve any two: [18]

a) Explain FH/BFSK modulation & demodulation system in detail.

b) Explain generation and properties of PN sequence.

c) Write short note on Ranging application using CDMA.

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Seat
No.

T.E. (Electronics-II) (Semester-VI)
Examination, May - 2017
ELECTRONIC SYSTEM DESIGN
Sub. Code : 66855

Day and Date : Saturday, 06-05-2017   Total Marks : 100
Time : 2.00 p.m. to 5.00 p.m.

Instructions :
1) Draw neat circuit diagram where ever necessary.
2) Clearly specify assumptions if any.
3) Numbers to right indicate full marks.
4) Write answers to bits in questions at one place and in sequence. Do not place answers randomly.
5) Answers to the bits written randomly may not be assessed.
6) Write answers neatly and should be legible.
7) Draw diagrams neatly and giving appropriate labels and legends.

SECTION-I

Q1) Answer the following.   **[18]**

a) What is reliability? Explain exponential law of reliability & factors for reliability of equipment.

b) Explain the concept of noise margin in various TTL and CMOS ICs.

c) Differentiate the characteristics of Op-Amps required to be used as an amplifier and a comparator.

Q2) Answer any two of the following.   **[16]**

a) What is the need of signal conditioning circuits in measurement or control application?

b) Design a floating load I to V convertor that will convert 4 to 20mA current signal into 0 to 8V ground referenced voltage signal.

c) Draw a neat circuit diagram and design a proportional controller to meet the following specifications:

Proportional band : 67%

Error max : ± 3

Full-scale output : 16V

Zero-error causes 25% controller output

P.T.O.

Q3) Answer any two of the following. [16]

    a) Describe how the touch point coordinates are detected in resistive touch pad (screen) technology?

    b) Draw and describe a circuit diagram showing details of a 10 bit serial ADC 12 C interface with 80C51 microcontroller. Choose and specify suitable pins of microcontroller for interface.

    c) A 10 bit ADC is supplied with reference voltage of 3.3V. What will be per bit (step) resolution of ADC? If this ADC is to be used to get output count in the range of 0 to 500 decimal, then what should be the range of input voltage analog voltage? Justify your answer.

SECTION-II

Q4) Solve any two. [16]

    a) With a neat diagram explain the ECG recording system.

    b) Explain types of ECG isolation circuits.

    c) Describe any one automatic drug delivery system with neat diagram.

Q5) Solve any two. [18]

    a) Discuss the switching buck (step-down) regulator. Derive the expression for output voltage.

    b) A SMPS with buck mode is used to regulate a output voltage to +15V. The supply input voltage rating from +27V to +102Volts. Find out the rating of transistor, diode, inductance and capacitance values, if maximum output (load) current is 1A.

    c) Design step-down SMPS regulator using LM3524 to regulate output voltage to +24V at load current to be 1A. The input voltage is varying from 5V to 7V.

Q6) Solve any two. [16]

    a) With a neat diagram explain time-domain EMI measurement system.

    b) Explain different types of shielding.

    c) Discuss various tests carried out on different products like FM radio, EEG machine, X-ray machine, PLC.

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Seat
No.

T.E. (Electronics Engineering) (Part-II) (Semester-VI) (Revised) Examination, May - 2017
POWER ELECTRONICS
Sub. Code : 66853

Day and Date : Tuesday, 02-05-2017   Total Marks : 100
Time : 2.00 p.m. to .5.00 p.m.

Instructions :   1)   All Questions are compulsory.
                 2)   Figures to the right indicate full marks.
                 3)   Assume suitable data if necessary.

Q1) Solve any three: **[18]**
     a)   Explain in detail class D turnoff method.
     b)   Define turn on time, reverse recovery time, gate recovery time related to SCR.
     c)   Explain dv/dt & di/dt protection circuit.
     d)   Explain out triggering ckt of SCR using PUT.

Q2) Solve any two: **[16]**
     a)   Explain in detail microprocessor based firing ckt for bridge controlled converter.
     b)   Explain single phase bridge converter with R load & also derive the equation of average & rms output voltage.
     c)   Assume UJT which has following specification at supply voltage 20V, rbb=6kΩ, I_B=4mA η=0.60, V_B=3V, I_p=2µA. Design UJT triggering ckt for SCR & also calculate pulse amplitude.

Q3) Solve any two: **[16]**
     a)   Explain in detail operation of single phase bridge converter with RLE load for continuous current mode of operation without free wheeling diode.
     b)   Derive the equation of source current of single phase bridge converter with R_L load for constant load current operators.
     c)   A single phase full converter supply to resistive load. Find the following performance parameter. For supply voltage=230V firing angle $\alpha = \pi/6$ R=5Ω. Find out.
         i)   Ave. o/p voltage   ii)   Supply rms current
         iii)   Supply fundamental current   iv)   Displacement factor

P.T.O.

Q4) Solve any two: [16]

a) Explain in detail class 'c' chopper.

b) Explain the operation of step down chopper with RL load also draw its o/p voltage, current waveform derive the equation of o/p voltage.

c) Chopper circuit is operated with chopping freq 1kHz on 220V dc supply. If required load voltage is 190V then calculate conduction period of switch in each cycle.

Q5) Solve any two: [16]

a) Explain in detail operation of single phase half bridge inverter with R load & also derive the equation of rms output voltage.

b) Explain in detail sine wave pulse width modulation for harmonic reduction in inverter.

c) A single phase bridge inverter supplies resistive load of 3 Ω and dc input voltage of 48V then calculate

   i)   Switch rating   ii) THD

   iii) Distortion factor   iv) Harmonic & distortion Factor of 20N

Q6) Solve any two: [18]

a) Explain servo type voltage stabilizer.

b) Explain in detail CVT.

c) Explain in detail single phase preventer.

d) Explain in detail block diagram of online & offline UPS.

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Seat No.

T.E. (Electronics) (Semester-VI) (Revised) Examination, May - 2017
COMPUTER ARCHITECTURE AND OPERATING SYSTEM-II

Sub. Code : 66854

Day and Date : Thursday, 4-05-2017   **Total Marks : 100**
Time : 2.00 p.m. to 5.00 p.m.

Instructions :   1)   All questions are compulsory.
                  2)   Figures to the right indicate full marks.
                  3)   Use suitable data if necessary.

SECTION-I

Q1) Answer any two.   [16]

   a)   Explain Booth's algorithm with example.

   b)   Draw and explain the flowchart for implementing twos compliment multiplier control unit.

   c)   Lists various types of operating system. Explain multiprocessor Operating system in details.

Q2) Attempt any Two.   [16]

   a)   Explain register level design of a floating point adder pipeline.

   b)   Design micro programmed control unit for twos compliment multiplier.

   c)   Explain the operating system services provided to user and to the system itself.

Q3) Attempt any three.   [18]

   a)   Explain hard wired control with example.

   b)   Explain the concept of multitasking.

   c)   Design 4 bit combinational Array Multiplier.

   d)   Write note on buffering and spooling.

P.T.O.

SECTION-II

Q4) Attempt any two. [18]

a) Explain the differences among short term, medium and long term process scheduling.

b) Distinguish between process and threads.

c) Explain process scheduling with the help of queueing diagram.

Q5) Attempt any two. [16]

a) What is deadlock? What are the necessary conditions for a deadlock to occur in a system?

b) Explain interprocess communication (IPC) mechanism of cooperating process using its message passing system model.

c) What is mutual exclusion? How it ensures that a race condition is avoided with it?

Q6) Attempt any two. [16]

a) Enlist page replacement algorithms. Describe FIFO algorithm in detail.

b) Explain page, frame and segment in detail.

c) Write a note on Logical, relative and physical addresses in memory management.

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Seat No.

T.E. (Electronics) (Semester - VI) (Revised) (New)
Examination, April - 2017
DIGITAL SIGNAL PROCESSING
Sub. Code : 66851

Day and Date : Wednesday,26-04-2017   Total Marks :100

Time : 2.00 p.m. to 5.00 p.m.

Instructions :
1) Figures to right indicate full marks..
2) Assume Suitable data if required.
3) All questions are compulsory.

SECTION - I

Q1) Attempt any Two.   **[18]**

   a) Compare DIT FFT and DIF FFT Algorithm.

   b) Explain in detail Overlap add methods of Sectioned Convolution.

   c) Determine the IDFT of $X(k) = \{3, (2+j), 1, (2-j)\}$.

Q2) Attempt any Two.   **[16]**

   a) Compare DFT and Wavelet Transform.

   b) Explain Various Properties of Wavelet Transform.

   c) Write a note on 'Applications of Wavelet Transform'.

Q3) Attempt any Two.   **[16]**

   a) Explain in detail designing FIR filter by Frequency Sampling Method.

   b) Design a FIR band stop filter to reject frequencies in the range of 1.5 kHz to 3 kHz and sampling frequency of 8 kHz with 7 samples using Fourier Series Method. Determine frequency response.

   c) Explain in detail design of FIR filter using windows.

P.T.O.

<u>**SECTION - II**</u>

Q4) Attempt any Two.   [18]

a)   Compare Impulse invariant Method and Bilinear Transformation Method.

b)   Write the procedure for the design of low pass digital Chebyshev IIR Filter.

c)   Write a note on 'frequency Transformation in IIR Filters'.

Q5) Attempt any Two.   [16]

a)   Explain in detail Architecture of TMS320C67XX.

b)   Write a note on 'finite word length effect in Digital filters'.

c)   Explain in detail various realization method of IIR filter.

Q6) Attempt any Two.   [16]

a)   Write a note on 'Sampling rate conversion by I/D factor'.

b)   Explain in detail Two Stage Interpolator.

c)   Explain in detail Applications of Multi-rate Digital filters.

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Seat No.

T.E. (Electronics) (Semester-V) (Revised) Examination, May - 2017
VLSI DESIGN
Sub. Code : 66283

Day and Date : Thursday, 18-05-2017   Total Marks : 100
Time : 10.00 a.m. to 1.00 p.m.

Instructions :
1) All questions are compulsory.
2) Figures to the right indicate full marks.
3) Assume suitable data if required.

SECTION-I

Q1) Attempt any THREE.   **[3x6=18]**

    a) Write a VHDL description to implement "xor gate" using 'When -else' statement.

    b) Explain the syntax with examples of Function, Procedure in VHDL.

    c) Write a VHDL description to implement 4:1 MUX using 'CASE' statement.

    d) Explain with example: 'Relational', 'Logical' and 'Shift' operators.

Q2) Attempt any TWO.   **[2x8=16]**

    a) Draw neat labeled diagram of 4 bit ripple carry adder and Write a VHDL description using structural architecture.

    b) Write a VHDL description to implement 4 bit shift register with left/right shift control input.

    c) How asynchronous inputs are interfaced with synchronous systems?

Q3) Attempt any TWO.   **[2x8=16]**

    a) Write a VHDL description for 8-bit wide 16 dip dual port RAM.

    b) Write a VHDL description for D F-F with

       i) Synchronous reset   ii) Asynchronous reset

    c) Explain with example Different types of architectures in VHDL.

P.T.O.

SECTION-II

Q4) Attempt any THREE. [3x6=18]

a) What is the need for simulation? Explain different types of Simulators.

b) Explain various ARRAY and DATA attributes.

c) What is testing and its need? Explain various fault models.

d) Explain different data transfer methods in datapath design.

Q5) Attempt any TWO. [2x8=16]

a) What are the inertial and transport delays? Explain with neat timing diagram. Write syntax for these.

b) Write a algorithm and design the datapath for n Factorial and list control words.

c) Design a control unit for simple IF - THEN - ELSE algorithm.

Q6) Attempt any TWO. [2x8=16]

a) With neat diagram explain boundary scan testing technique.

b) Explain with neat diagram structure of IOB of XC95xx series CPLD.

c) List various features of Spartan - II FPGS and details of BLOCK RAM.

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Seat No.

T.E. (Electronics Engineering) (Part - II) (Semester - VI) (Revised) Examination, April - 2017
VIDEO ENGINEERING
Sub. Code : 66852

Day and Date : Friday,28-04-2017   **Total Marks :100**

Time : 2.00 p.m. to 5.00 p.m.

Instructions : 1) All questions are compulsory.
2) Use suitable assumptions if required.
3) Draw necessary figures on right side of answer sheet.

SECTION - I

Q1) Solve any three.   **[18]**

a) Draw the block diagram of PAL encoder and write function of each block.

b) Draw constructional details of Plumbicon camera tube and describe its working.

c) Why AM is preferred for picture signal transmission and FM for sound signal transmission.

d) Define the following terms related to T.V. systems.

i) Aspect ratio.

ii) Hue.

iii) Contrast.

iv) Brightness.

e) Illustrate concept of optical recording, with relevant diagram.

P.T.O.

Q2) Solve any two. [16]

    a) Why interlace scanning is necessary in TV system? Explain interlace scanning in brief.

    b) Explain compatibility considerations along with frequency interleaving.

    c) Compare PAL and NTSC T.V. system.

Q3) Solve any two. [16]

    a) Explain VSB transmission and channel bandwidth.

    b) How phase error is eliminated in PAL system.

    c) Explain construction and working of any one type of Microphone and Speaker.

SECTION - II

Q4) Attempt any Three sub Questions. [18]

    a) Draw and Explain the Multiplexed Analog Component encoding format used for transmitting colour Television Signals.

    b) Draw & Explain the block schematic of the signal flow in video codec and the video processor.(ITT).

    c) Draw the structure of the plasma display panel (PDP) used for television and explain its working.

    d) Explain with suitable block diagram DTH television receiver.

Q5) Attempt any Two sub Questions. [16]

    a) Draw and explain D_2MAC Baseband signal waveform for normal unscrambled picture transmission.

    b) Explain passive Matrix display. What are the disadvantages of it? Explain how that are overcome by active matrix liquid crystal display.

    c) Explain in case of satellite T.V.

        i) Geostationary orbit.

        ii) Transponder.

Q6) Attempt any Two sub Questions. [16]

a) Draw the Block diagram of the Deflection processor DPU 2553 (ITT) and Explain the digital signal processing carried out in it.

b) With neat block diagram explain the working of IR remote control used for Television.

c) Describe the main merits and applications of CATV system. Draw a typical layout of this system of signal distribution and label all the blocks. Why are the amplifiers and equalizers required along trunk distribution lines?

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Seat No.	

T.E. (Electronics) (Semester-V)
Examination, May - 2017
SIGNALS & SYSTEMS
Sub. Code : 66280

Day and Date : Monday, 15-05-2017

Time : 10.00 a.m. to 1.00 p.m.

Total Marks : 100

Instructions :   1)   All Questions are compulsory.
　　　　　　　　2)   Figures to the right indicate full marks.
　　　　　　　　3)   Assume necessary data wherever required.

SECTION-I

**Q1)** Solve any two.　　　　　　　　　　　　　　　　　　　　　　　　**[16]**

　　a)　Draw even and odd parts of following signals.

　　　　i)　$x(t) = \sin(t) + 2\sin(t) + 2\sin^2(t) \cdot \cos(t)$

　　　　ii)　$x[n] = [-2, 1, \underset{\uparrow}{2}, -1, 3]$

　　b)　Find the convolution integral of the following signals and plot resultant sketch.

　　　　$x(t) = 1$　for $0 \le t \le 4$ and $h(t) = 0 \le t \le 1$
　　　　$= 0$ Elsewhere　　　　　　　$=$ Elsewhere

　　c)　Determine whether the following LTI systems are causal or not.

　　　　i)　$h(t) = e^{-3t} \cdot u(t-1)$　　　　ii)　$h[n] = (0.5)^n \cdot u[n+3]$

Q2) Solve any two.　　　　　　　　　　　　　　　　　　　　　　　　**[16]**

　　a)　Determine whether the following signals are energy signal, power signal or neither of two.
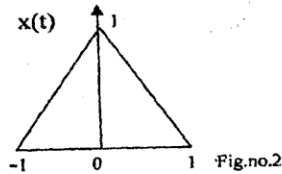
　　　　i)　$x(t)$

Fig.no.1

　　　　ii)　$x[n] = (-0.5)^2 u[n]$

P.T.O.
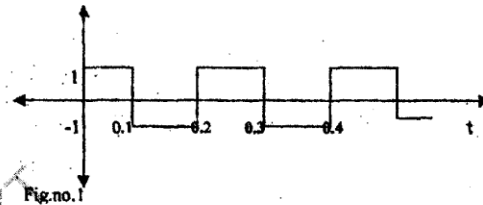
b) Find the convolution sum of the following signals and find values for n=-5, n=5 and n=10.

$$x[n]= u[n] \text{ and } h[n]= (\frac{3}{4})^n u[n]$$

c) A signal x(t) is as shown in fig.no.2 sketch and label each of the following.

Fig.no.2

i) $x(2(t+2))$ ii) $x(3t+2)$

iii) $x(-2t-1)$ iv) $x(3t)+x(3t+2)$

Q3) Solve any three.   **[18]**

a) State and explain sampling theorem.

b) With a neat schematic explain aliasing effect.

c) Determine whether the following signals are periodic or non periodic. If periodic find fundamental period.

i) $x[n] = \cos[\frac{\pi n}{2}]-\sin[\frac{\pi n}{8}] + 3\cos[\frac{\pi n}{4}+\frac{\pi}{3}]$

ii) $x(t) = 2\cos(t) + \sin(\sqrt{3}t)$

d) Define and explain all properties of systems.

SECTION-II

Q4) Attempt any two.   **[16]**

a) Determine the Z Transform and ROC of the following finite duration signals:

i) $X[N] = \{1,2,3,5,-1,-2,-3\}$

$$\uparrow$$

ii) $X[n] = \{0,5,10,15,20\}$

iii) $X[n] = \delta[n-2] + \delta[n+2]$

b) Show that DTFT is periodic with period 2π. Discuss convolution property of DTFT?

c) Compute Fourier Transform of $x(t) = (t+4)e^{-2(t+4)} u(t+4)$?

Q5) Attempt any two. [16]

a) Discuss and derive following properties of Z Transform:

   i) Convolution theorem   ii) Scaling theorem

   iii) Time reversal   iv) Time shifting

b) Find Inverse Z-Transform of

$$X(Z) = \frac{\frac{1}{4}Z^{-1}}{(1-\frac{Z^{-1}}{2})(1-\frac{Z^{-1}}{4})} \text{ with ROC } \frac{1}{4}<|Z|<\frac{1}{2}$$

c) Compute four point DFT of $x[n] = \{3,-1,2,0\}$ using DFT equation?

Q6) Attempt any two. [18]

a) Compute the transfer function of the system and realize it in Direct Form -1 and II:

$$y[n] + \frac{1}{4} y[n-1] - \frac{1}{8} y[n-2] = -2 x[n] + \frac{5}{4} x[n-2]$$

b) Compute IDFT of $X(k) = \{0,1-j,2,1+j\}$

c) Discuss linear constant coefficient differential equation for continuous time system? Obtain a differential equation for a series RLC circuit?

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Seat No.

T.E. (Electronics) (Semester-V)
Examination, May - 2017
ELECTROMAGNETIC ENGINEERING
Sub. Code : 66282

Day and Date : Wednesday, 17-05-2017　　　　　　　Total Marks : 100
Time : 10.00 a.m. to 1.00 p.m.

Instructions :　1)　All questions are compulsory.
　　　　　　　　2)　Figures to the right indicate full marks.
　　　　　　　　3)　Assume suitable data if necessary.
　　　　　　　　4)　Use of non-programmable calculator is allowed.
　　　　　　　　5)　Use Smith chart if necessary.

SECTION-I

Q1) Attempt any two.　　　　　　　　　　　　　　　　　　　　**[16]**

　　a)　Derive the expression for divergence theorem.

　　b)　Explain the concept of electric dipole & dipole moment; derive the expression for electric potential due to electric dipole.

　　c)　Given the electric flux density, $D = 4xy a_x + 2(x^2+z^2)a_y + 4yza_z$ C/m^2, Use Gauss's law. Determine total charge enclosed in the rectangular parallelopiped formed by $0 \le x \le 2, 0 \le y \le 3, 0 \le z \le 5m$.

Q2) Attempt any two.　　　　　　　　　　　　　　　　　　　　**[16]**

　　a)　Given the vectors $M = -10a_x + 4a_y - 8a_z$ & $N = 8a_x + 7a_y - 2a_z$, find:

　　　　i)　$-M + 2N$　　　　　ii)　Unit vector in the direction of $-M + 2N$

　　　　iii)　$N - 3M$,　　　　　iv)　Magnitude of $5ax + N - 3M$

　　b)　Evaluate both sides of Stoke's theorem for the field $H = 6xya_x - 3y^2a_y$ A/m and the rectangular path around the region, $2 \le x \le 5, -1 \le y \le 1, z = 0$ (Positive direction of ds be a_z).

　　c)　Obtain the expression for magnetic field intensity H at point p due to infinite length filament which carries current of I ampere.

P.T.O.

Q3) Attempt any three. [18]

    a) Write a short note on Cartesian, cylindrical & spherical coordinate systems.

    b) Explain the concept of Scalar electric potential.

    c) If $V = 2xy^2z^3$ Given point P(1, 2, −1), find:
        i)   V at P;   ii)   E at P.

    d) A point charge Q=18nC has velocity of 5×10^6 m/s in the direction $a_r=0.04a_x+0.05a_y+0.2a_z$. Calculate the magnitude of the force exerted on the charge by the field,
        i) $E = -3a_x+4a_y+6a_z$ KV/m;   ii) $B= -3a_x+4a_y+6a_z$ mT

SECTION-II

Q4) Solve any Two. [16]

    a) What is polarization of wave? With neat diagram explain linear, circular and elliptical polarization.

    b) What is inconsistency in ampere's law? Explain.

    c) Find the reflection coefficient and transmission coefficient of an electric field wave travelling in air and incident normally on a boundary between air and dielectric having permeability μ_0 and permittivity $\varepsilon_r=4.74$.

Q5) Solve any Two. [16]

    a) Explain in detail various transmission line parameters.

    b) The parameters of certain transmission line operating at 6×10^8 rad/s are L=0.4 μH/m, C=40 pF/m. G= 80 μS/m, and R = 20 ohm/m. Find α, β, λ and Zo.

    c) Give Maxwell's equations for time varying fields.

Q6) Solve any three. [18]

    a) Poynting Theorem

    b) Smith chart

    c) Wave equations for sinusoidal time variations

    d) Polarization

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Seat No.

**T.E. (Electronics Engg.) (Part - I) (Semester - V) (Revised)
Examination, May - 2017
MICROCONTROLLERS
Sub. Code : 66281**

Day and Date : Tuesday, 16 - 05 - 2017   **Total Marks : 100**
Time : 10.00 a.m. to 1.00 p.m.

Instructions :   1)   **All questions are compulsory.**
                  2)   **Assume suitable data if necessary.**
                  3)   **Figures to the right indicate full marks.**

SECTION - I

Q1) Answer <u>Any 4</u> of the following: (5 Marks Each)   **[20]**

   a)   Draw a core architecture of 8051.

   b)   Compare between 89c52 and 89c420 Microcontrollers.

   c)   Explain the IE SFR with its format.

   d)   Explain the rotate left instructions of 8051 with suitable example.

   e)   Draw port-0 internal structure and explain it briefly.

Q2) Answer <u>Any two</u> of the folloing: (8 Marks Each)   **[16]**

   a)   Write ASM code to find smaller of 10 numbers stored in IRAM & keep answer in XRAM.

   b)   Explain the power saving modes of MCS-51 with suitable diagram.

   c)   Explain the Timer/Counter mode-2 of 8051 with suitable diagram.

P.T.O.

Q3) Answer <u>Any two</u> of the following: (7 Marks Each) **[14]**

a) Write ASM code to Transmit the block of data (15 characters) stored at IRAM serially at 9600 baud using On-chip UART Port of 8051. (assume crystal frequency = 12 MHz.)

b) Draw and explain interfacing of keypad to 8051.

c) Draw a hardware interface of common anode character display to 8051 and explain it in brief.

SECTION - II

Q4) Answer any THREE from the following (6 marks each): **[18]**

a) Explain 'Memory Types' used in Embedded - C for 8051.

b) Explain different alternate multiplexed pin functions of PORTA of 16F877.

c) Describe CAPTURE mode of CCP module.

d) Explain following instructions of 16F877.

    i) ADDWF f,d

    ii) CALL k

Q5) Answer any TWO from the following (8 marks each): **[16]**

a) Write an Embedded - C program for 8051, for SUBTRACTION of data bytes received through ports. Use P0 & P1 as input ports to receive data. Send the result to port P2.

b) Explain the Serial Peripheral Interface (SPI) mode of MSSP Module.

c) Draw format and explain different bits of OPTION_REG register.

Q6) Answer any TWO from the following (8 marks each): **[16]**

a) Write a PIC 16F877 assembly language program to generate a square wave on port D using software delay.

b) Draw and explain Direct/Indirect addressing using INDF and FSR Registers.

c) Draw and explain block diagram of ADC feature of PIC 16F877.

Seat
No.

**T.E. (Electronics) (Pre-revised) (Part - III) (Semester - V)
Examination, May - 2017
CONTROL SYSTEM ENGINEERING
Sub. Code : 45593**

Day and Date : Thursday, 18 - 05 - 2017   Total Marks : 100
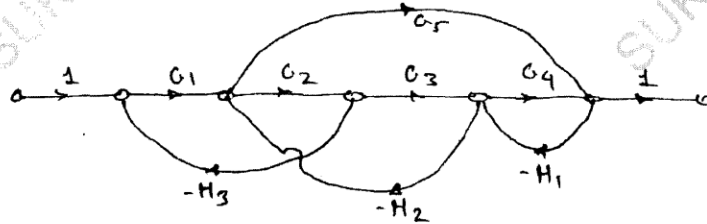Time : 10.00 a.m. to 01.00 p.m.
Instructions :   1)   All the questions are compulsory.
                  2)   Assume suitable data if necessary.

SECTION - I

Q1) Solve any two of the following :   [2×9=18]

   a)   State and explain rules for Block diagram reduction technique.

   b)   Obtain the Transfer Function for Signal Flow Graph shown in figure.

   c)   Derive transfer Function of field controlled DC servo motor.

Q2) Solve any two of the following :   [2×8=16]

   a)   Derive steady state error for type zero, type one & type two system
        when ramp input is given.

   b)   Derive any two Time Domain Specifications.

c)   The control system having unity feedback has

$$G(S) = \frac{10(s+1)}{s(s+2)(s+5)}$$

Determine k_p, k_v & k_a

Q3) Solve any two of the following :   [2×8=16]

a)   Draw Root Locus for the system.

$$G(s).H(s) = \frac{k}{s(s+2)(s+5)}$$

b)   Explain advantage of closed loop system over open loop system.

c)   Explain in brief effect of disturbance signals by use of feedback.

SECTION - II

Q4) Solve any two of the following :   [2×9=18]

a)   Explain steps to solve Nyquist Plot. Also explain Gain Margin & Phase Margin.

b)   For the system having open loop transfer function

$$G(s).H(s) = \frac{10}{s(s+1)(s+10)}$$

Determine the stability of the system by plotting Bode Plot of the system.

c) Find the Transfer function of the system

$$A = \begin{bmatrix} 0 & 1 & 0 \\ 0 & 0 & 1 \\ -2 & -4 & -6 \end{bmatrix} \quad B = \begin{matrix} 0 \\ 0 \\ 1 \end{matrix} \quad C = \begin{bmatrix} 1 & 1 & 0 \end{bmatrix} \quad D = 0$$

Q5) Solve any two of the following :   [2×8=16]

a) With help of neat circuit diagram explain the PD Controller.

b) Solve Polar Plot

$$G(s).H(s) = \frac{100}{(s+2)}$$

c) Explain effect of addition of poles & zeros on stability of the system.

Q6) Solve any two of the following :   [2×8=16]

a) With neat sketch Derive Lag Compensator.

b) Find controllability and observability.

$$A = \begin{bmatrix} 1 & -1 \\ 1 & -1 \end{bmatrix} \quad B = \begin{matrix} 0 \\ 1 \end{matrix} \quad C = \begin{bmatrix} 1 & 0 \end{bmatrix}$$

c) Classify time domain analysis & frequency domain analysis.

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